THE ANALYSE OF BUTLER OSCILATOR AND POWER DISSIPATION IN THE CRYSTAL UNIT

Zdeněk Roubal

Doctoral Degree Programme (3), FEEC BUT

E-mail: roubalz@feec.vutbr.cz

Supervised by: Miloslav Steinbauer

E-mail: steinbau@feec.vutbr.cz

Abstract: In many applications, for example a direct digital synthesis, it is necessary to use the high quality and on higher overtone working crystal oscillator. One of the best circuits for this purpose is Butler oscillator as emitter follower. By this circuit is possible to design a high frequency oscillator working up to hundred megahertz. In this paper the design of the Butler oscillator at 2^{26} Hz by use of a feedback loop analysis in resonance frequency vicinity of the crystal is showed. Influence of the circuit elements values is calculated in Matlab environment. This is important for low phase noise (high short-term stability) oscillator design and stability of the output signal amplitude. The design is oriented on the maximum short-term stability. The next step is determination and optimalization of the power dissipation in the crystal unit. For decreasing of this power dissipation we use limiting diodes.

Keywords: Butler oscillator, DDS source of clock signal, piezoelectric crystal unit, harmonic balance, Matlab

1. INTRODUCTION

Direct digital synthesis is used in many applications. There is necessary to use a quality source of the clock signal. In these special applications, output frequency need to be whole number. This is a problem in the DDS because the output frequency is given by equation

$$f_{\mathrm{OUT}} = \frac{M \cdot f_{\mathrm{REF}}}{2^n} \tag{1}$$

f_{out} is output frequency, M is tuning word and n is tuning word with (in bits). Frequency of the clock signal source has to be equal to power number two. The next condition is a high long-term stability and low phase noise. Crystal oscillators perfectly meet these conditions. Tab. 1 shows parameters of the cut AT Piezoelectric crystal which is frequently used [1]. In the Fig. 1 is equivalent circuit [1].

Overtone	Frequency range [MHz]	R_{hn} [Ω]
1st	1,6 – 22	500-25
3rd	16 - 66	40-35
5th	30 – 160	50-65
7th	90 – 190	100-120
9th	120 - 190	130

Tab. 1 Equivalent series resistance Piezoelectric crystal unit[1]

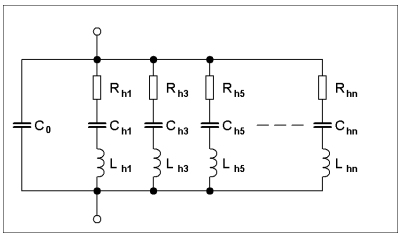

Fig. 1 Equivalent circuit crystal unit

Some integrated circuit DDS [2] has internal multiplayer referenced which use a phase lock loop. In this case the output phase noise will be worse. For critical applications where we

require higher output frequency is necessary to use crystal oscillator oscillating on an overtone of the piezoelectric crystal unit.

2. BUTLER OSCILLATOR

One of the most used crystal oscillator is Butler oscillator oscillating on overtone of the piezoelectric crystal unit [3], [4]. There are two types of these circuits. The first type use a transistor operates with common base (Fig. 2). In second case transistor operates as an emitter follower (Fig. 3). More used Common base Butler oscillator has higher output power but its adjusting is critical. Increasing of the collector direct current will increase transconductance of the transistor and also increase gain margin to keep oscillation conditions. In consequence, input impedance of the transistor is decreasing and it can cause the capacitive divider inhibiting. This circuit can generate various spurious oscillations. On the other hand Butler oscillator as emitter follower has less critical adjusting and has no spurious oscillations [3]. Disadvantage is lower output power.

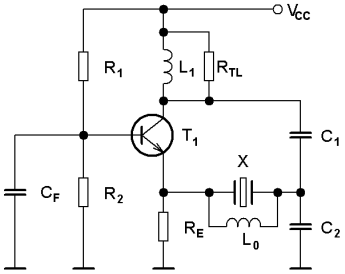

Fig. 2 Common base Butler oscillator

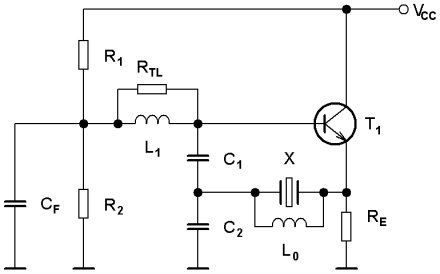

Fig. 3 Butler oscillator as emitter follower

For alternative signal is inductance L_1 grounded by using filter capacitor C_F. Transistor T_1 must meet sophisticated requirements. It is necessary that its transition frequency f_T has to be 10x higher than oscillation frequency [3]. Consequently, phase shift caused by transistor will be negligible and we can minimize influence of the transistor on stability of the oscillation frequency. Parasitic capacities of the electrodes of the transistor and capacity of its semiconductor junctions, especially junction base-emitter, need to be minimal for influence reduction on oscillation condition. The next requirement is minimal noise 1/f. Manufacturer usually does not guarantee this requirement. This noise increases the phase noise of the crystal oscillator and also causes worse short frequency stability [5].

3. ANALYZE FEEDBACK CIRCUIT

For easier understanding of the feedback circuit component design (Fig. 4) is suitable to use voltage transfer of the feedback circuit. Inductance L_0 with static capacitance C_0 is tuned to resonance so these components are possible to neglect. If resistor R_E has value which is several times higher than output emitter follower impedance so is possible to neglect it. Otherwise, is possible to connect it in parallel to output impedance. Output Impedance R_{out} of the emitter follower we will think as real because transition frequency f_T is several times higher. Consequently, output impedance is included to total resistance: $R_T = R_{hn} + R_{out}$.

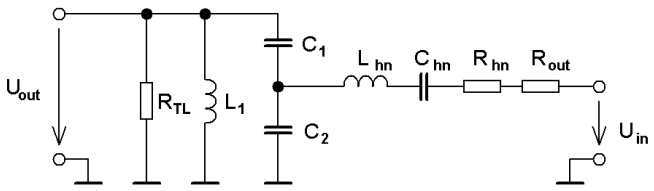

Fig. 4 Feedback circuit

Voltage transfer of the feedback circuit was calculated in SNAP program. The final result is:

$$A = C_1 \cdot C_{hn} \cdot L_1 \cdot R_{TL}$$
$$B = R_{TL} \cdot C_{hn} + R_{TL} \cdot C_1 + R_{TL} \cdot C_2$$
$$C = C_1 \cdot L_1 + C_2 \cdot L_1 + C_1 \cdot C_{hn} \cdot R_T \cdot R_{TL} + C_2 \cdot C_{hn} \cdot R_T \cdot R_{TL} + C_{hn} \cdot L_1$$
$$D = C_2 \cdot C_1 \cdot L_1 \cdot R_{TL} + C_1 \cdot C_{hn} \cdot L_1 \cdot R_{TL} + C_2 \cdot C_{hn} \cdot L_{hn} \cdot R_{TL} + C_1 \cdot C_{hn} \cdot R_T \cdot L_1 + C_2 \cdot C_{hn} \cdot R_T \cdot L_1 + C_1 \cdot C_{hn} \cdot L_{hn} \cdot R_{TL}$$
$$E = C_2 \cdot C_1 \cdot C_{hn} \cdot R_T \cdot L_1 \cdot R_{TL} + C_2 \cdot C_{hn} \cdot L_{hn} \cdot L_1 + C_1 \cdot C_{hn} \cdot L_{hn} \cdot L_1$$
$$F = C_2 \cdot C_1 \cdot C_{hn} \cdot R_T \cdot L_1 \cdot R_{TL}$$
$$K_U(s) = \frac{s^2 \cdot A}{B + s \cdot C + s^2 \cdot D + s^3 \cdot E + s^4 \cdot F}$$

For required frequency f_0=2^{26} Hz was manufactured piezoelectric crystal unit working on the serial resonance with parameters R_{h5}=50 Ω , C_{h5}=1 fF , C_0=6,02 pF , f_{s5}=2^{26} Hz. The piezoelectric crystal unit is used on 5th overtone. Initial values of the feedback circuit were chosen according to literature [3]: Modulus impedance C_2 has same or smaller value as R_h, L_1 was chosen from E12 series 220 nH, C_1 and L_1 are approximately in resonance, quality Q of the coil L_1 is cut by 10 by R_{TL}. Inductance L_0 and capacitor C_0 are in resonance.

$C_2 \geq 47\ pF \qquad L_1 = 220nH \qquad C_1 = 26\ pF \qquad R_{TL} = 1\,k\Omega \qquad L_0 = 1{,}02\ \mu H$

As transistor was chosen BFR92A with f_T=4 GHz. Minimum noise is guaranteed by manufacturer with current I_C=5 mA. Output impedance is determined from S-parameters declared by manufacturer as:

$$Z_{OUT} = \left(y_{22} - \frac{y_{12} \cdot y_{21}}{y_{11} + Y_G} \right)^{-1} = (5{,}1492 + 0{,}9281\,j)\,\Omega \qquad (1)$$

Imaginary part of the output impedance will slightly influence the oscillation frequency. Real part is included to R_T. The amplitude frequency characteristic of the feedback circuit is in Fig. 5, phase characteristic is in Fig. 6. This consecution is assumed from [3]. The parameter is the resistance R_{TL}, the other components have initial value. In the figure is showed that with decrease of the value R_{TL} is gain margin decreasing and slope when a phase curve is crossing the zero value is increasing.

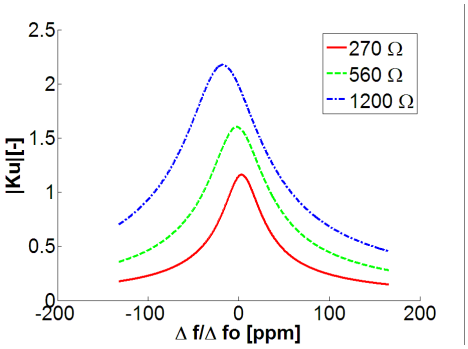

Fig. 5 Amplitude frequency characteristic for parameter R_{TL}

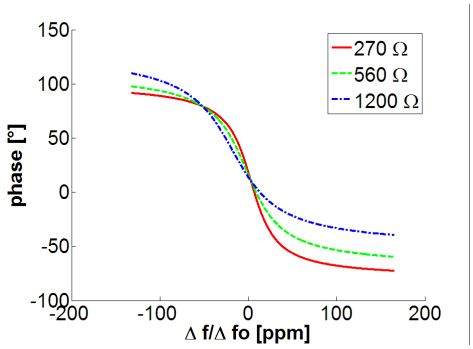

Fig. 6 Phase frequency characteristic for parameter R_{TL}

If the phase shift feedback circuit is zero the oscillation condition will be realized. Here is neglect phase shift in transistor. The plan is to attain higher slope of characteristic transit phase characteristic zero. In the next step were established conditions on oscillation frequency for varying value C_1 and several values R_{TL}. This consecution is new in my paper. In the Fig. 7 is depended voltage transfer |*K*u| in realized oscillation condition. In the Fig. 8 is difference phase for detuning 5ppm around oscillation frequency. In the Fig. 9 is rate variation oscillation frequency to series resonance frequency piezoelectric crystal unit.

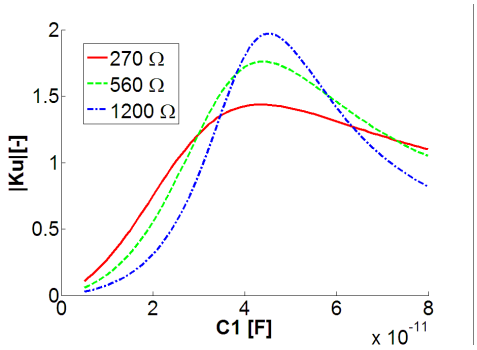

Fig. 7 $|K_u|$ in realized oscillation condition for parameter R_{TL}

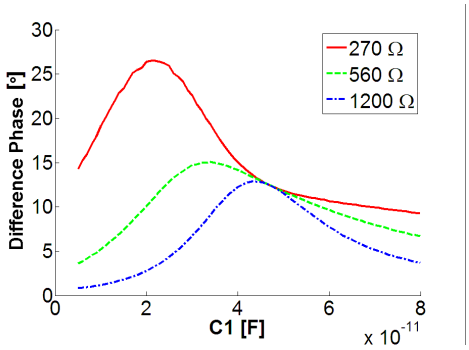

Fig. 8 Difference phase for detuning 5ppm around oscillation frequency

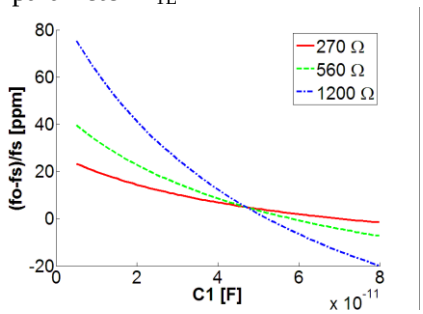

Fig. 9 Rate variation oscillation frequency to series resonance frequency PKJ for parameter R_{TL}

For R_{TL}=270 Ω was chosen value C_1=31 pF for maximum slope of phase curve (Fig. 8) and $|Ku|$ in realized oscillation condition larger than one. Circuit with optimum value was simulated in Ansoft Designer and whereby harmonic balance [6] was determined the amplitude of the harmonics in output oscillator (Fig. 10). In the Fig. 11 is phase noise for optimal design.

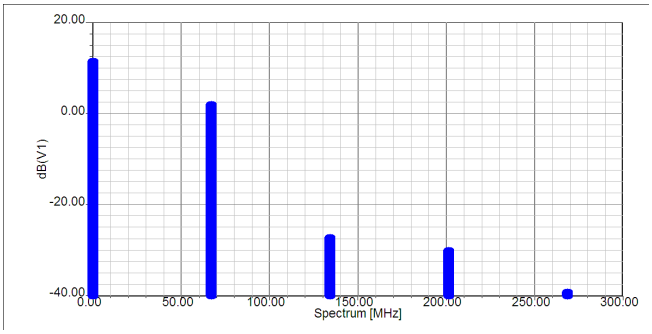

Fig. 10 Spectrum output signal

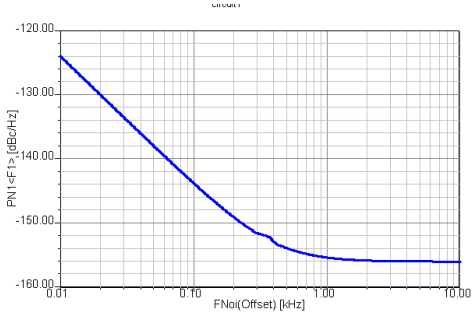

Fig. 11 Phase noise

4. POWER DISSIPATION IN THE CRYSTAL UNIT

Power dissipation in the crystal unit influences its resonance frequency. For long-term stability is necessary to observe the maximum value of power dissipation guaranteed by manufacturer and keep this value lower. In the program Ansoft designer was determined the optimal value of the circuit components for power dissipation in the crystal unit. The parameter is the R_{TL} value. In the Fig. 14 is dependence of the power dissipation circuit in the crystal unit on R_{TL}. Its value is too large. For its decrease are used limiting diodes which are in antiparallel to coil L_1, according to [3]. In the Fig. 13 is shown the time scope of voltage in L_1 without limiting diode. The vf schottky dual diode HSMS-2822 were used because normal silicon diode have a large threshold voltage. In the Fig. 15 is dependence of the power dissipation circuit in the crystal unit on R_{TL} with limiting diode. These dependences are difficult to measure. This simulation is important for design of the Butler oscillator and was not published in the literature.

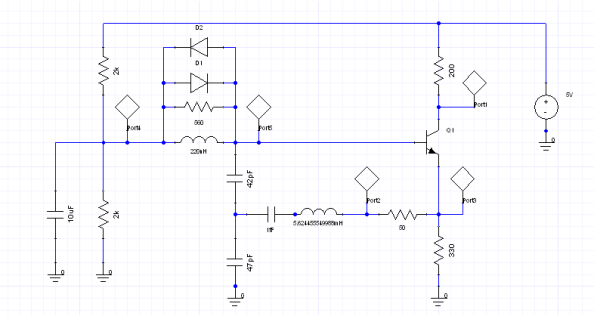

Fig. 12 Simulation circuit in Ansoft designer with dual diode HSMS-2822

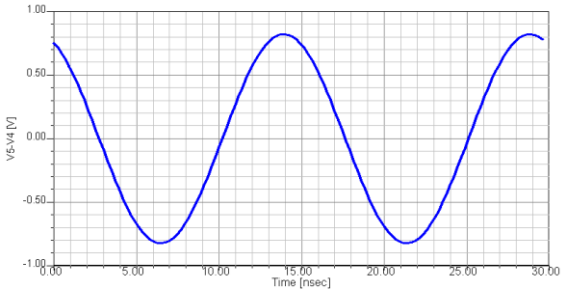

Fig. 13 Time scope of voltage in R_{TL} for R_{TL}=560 Ω

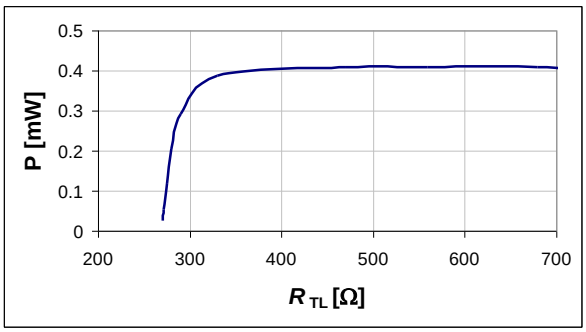

Fig. 14 Power dissipation in the crystal unit without limiting diodes

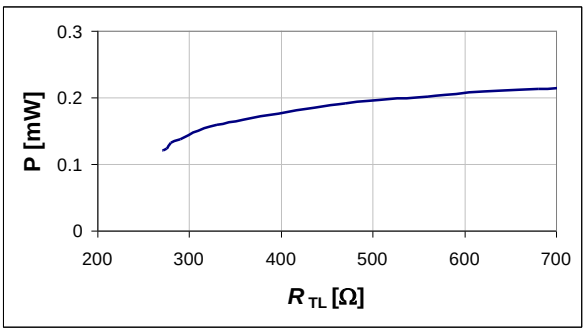

Fig. 15 Power dissipation in the crystal unit with dual diode HSMS-2822

5. CONCLUSION

For required frequency, the feedback circuit optimized for the maximum short-term frequency stability and lower phase noise was designed. Reduction of R_{TL} value is causing increase of the frequency stability of the oscillator and decrease of the gain margin. Piezoelectric crystal unit was manufactured with modified serial resonance frequency, 9.9 ppm under required oscillation frequency. For limiting of the output signal and for decreasing the Power dissipation in the crystal unit is used the dual diode HSMS-2822, the phase noise increase is negligible.

ACKNOWLEDGEMENT

The research described in the paper was financially supported research plans MSM 0021630513, MSM 0021630516 of the Ministry of Education, Youth and Sports of the Czech Republic and project of the BUT Grant Agency FEKT-S-11-5.

REFERENCES

[1] Zelenka, J.: Piezoelektrické rezonátory a jejich použití. Academia, 1983.

[2] A technical Tutorial on Digital Signal Synthesis. [Online]. Analog Devices, Inc., 1999 - [cit. 20.2. 2011]. Dostupné na http://www.ieee.li/pdf/essay/dds.pdf

[3] Matthys R., J.: Crystal oscillators circuit. Krieger Publishing Company, 1991.

[4] Frerkin, M.: Crystal Oscillator Design and Temperature Compensation. New York: Van Nostrand Reinhold Company, 1978.

[5] Šojdr, J.: Krátkodobá stabilita kmitočtu krystalového oscilátoru. Sborník přednášek Elektronické a piezoelektrické prvky a obvody, 1983.

[6] Odyniec, M.: RF and Microwave Oscillator Design. Boston: Artech House, 2002.